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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Mikio TANAKA, et al.	Examiner:	Unassigned
Serial No.:	Unassigned	Group Art Unit:	Unassigned
Filed:	Herewith	Docket:	14457
For:	MEMORY LSI FAILURE ANALYSIS APPARATUS AND ANALYSIS METHOD THEREOF		Dated: March 28, 2001



**Assistant Commissioner for Patents
Washington, DC 20231**

INFORMATION DISCLOSURE STATEMENT

Sir:

In accordance with 37 C.F.R. §§1.97 and 1.98, it is requested that the following references, which are also listed on the attached Form PTO-1449, be made of record in the above-identified case.

1. Japanese Application Publication No. 2629523, dated April 18, 1997;
2. Japanese Application Publication No. 11-306793, dated November 5, 1999;
3. Japanese Application Publication No. 2000-200814, dated November 18, 2000;
4. Japanese application Publication No. 2000-321333, dated November 24, 2000;

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I hereby certify that this correspondence is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 C.F.R. § 1.10 on the date indicated above and is addressed to the Assistant Commissioner for Patents and Trademarks, Washington, D.C. 20231 on March 28, 2001.

Dated: March 28, 2001

Janet Grossman

5. Japanese Application Publication No.2000-21195, dated January 21, 2000; and
6. Japanese Application Publication No. 2000-187062, dated July 4, 2000.

Applicants are submitting copies of the above-cited references. The relevance of the above-identified references has been described in the specification.

Inasmuch as this Information Disclosure Statement is being submitted in accordance with the schedule set out in 37 C.F.R. § 1.97(b), no petition, certification or fee is required.

Respectfully submitted,



Paul J. Esatto, Jr.
Registration No.: 30,749

Scully, Scott, Murphy & Presser
400 Garden City Plaza
Garden City, New York 11530
(516) 742-4343

PJE:AHS